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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,180	12/02/2003	Simon Robert Walmsley	PEA15US	4589

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
TRUVAN, LEYNNA THANH	
ART UNIT	PAPER NUMBER
2135	
MAIL DATE	DELIVERY MODE
04/07/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,180	WALMSLEY ET AL.	
	Examiner	Art Unit	
	Leynna T. Truvan	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/17/2008 has been entered.

Response to Arguments

3. Applicant's arguments, see ***RCE***, filed ***1/17/2008***, with respect to the rejection(s) of ***claim(s) 1-3 under 35 U.S.C. 103(a) as being unpatentable over Gilbert, et al. in view of O'Donnell, et al.*** have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of ***Gilbert, et al. and Rager, et al.***

Gilbert discloses the invention that provides hardwired logic or microprocessor integrated circuit chips with protection against fraud (Gilbert-col.1, lines 10-15), but did not go into details of a tamper detection line arranged to obscure operation of the non-volatile memory. Rager discloses an invention that provides a method and apparatus for greater security in storing and utilizing encryption/decryption keys in a non-volatile memory where the placement of keys in the EEPROM inherently causes risks. Thus, to provide maximum key security the

communication unit must be protected against tampering by an adversary with a tamper loop and tamper detect circuit where the tamper loop is an electrical path that must be broken in order to physically access any device containing key information (Rager-col.3, line 63 – col.4, line 7). Therefore, it would have been obvious for a person of ordinary skills in the art to at the time the invention was made to include a tamper detection line arranged to obscure operation of the non-volatile memory to the integrated circuit chips of Gilbert in view of the teachings of Rager because provide maximum key security the communication unit much be protected against tampering by an adversary (Rager – col.3, line 63 – col.4, line 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert, et al. (US 7,165,177), and further in view of Rager, et al. (US 5,457,748).

As per claim 1:

Gilbert discloses a plurality of integrated circuits, each of the integrated circuits **(col.1, lines 13-14 and col.4, lines 14-15)** comprising a processor and non-volatile memory **(col.5, lines 39-40 and col.7, lines 41-53)** *[and a tamper detection line arranged to obscure operation of the non-volatile memory]*, and including code for running identical software processes, wherein each of the integrated circuits also includes secret information used by the software process **(col.2, lines 4-10 and col.6, lines 11-14; *secret information can broadly interpret as data that is protected and secure such that may involve authentication***

or verification process. Gilbert's secret key, authentication data, or certificate value (col.3, lines 1-28) which is referring to the claimed secret information.), the secret information in each chip being located in a different location in the memory relative to a plurality of the other chips. **(col.6, lines 18-22 and col.7, lines 55-65)**

Although, Gilbert discloses the invention that provides hardwired logic or microprocessor integrated circuit chips with protection against fraud (col.1, lines 10-15), where tamper detection involves protection against fraudulent transactions. However, Gilbert did not go into details of a tamper detection line arranged to obscure operation of the non-volatile memory.

Rager discloses an invention that provides a method and apparatus for greater security in storing and utilizing encryption/decryption keys in a non-volatile memory such as EEPROM (col.2, lines 32-38). There includes a microcontroller, encryptor, and decryptor that may comprise either a single or separate IC devices (col.2, lines 60-63). Rager discloses the placement of keys in the EEPROM inherently causes risks, thus to provide maximum key security the communication unit must be protected against tampering by an adversary. This is accomplished with a tamper loop and tamper detect circuit where the tamper loop is an electrical path that must be broken in order to physically access any device containing key information. If an attempt is made to dissemble or tamper with the communication unit, the tamper circuit will trigger the microcontroller to erase the key stored in the decryptor (col.3, line 63 – col.4, line 7).

Therefore, it would have been obvious for a person of ordinary skills in the art to at the time the invention was made to include a tamper detection line arranged to obscure operation of the non-volatile memory to the integrated circuit chips of Gilbert in view of the teachings of

Rager because provide maximum key security the communication unit much be protected against tampering by an adversary (Rager – col.3, line 63 – col.4, line 7).

As per claim 2: see Gilbert on col.6, lines 18-22 and col.7, lines 55-65; discussing a plurality of integrated circuits according to claim 1, wherein the code on each integrated circuit is such that the software process of each chip knows the location in memory via which the secret information is accessible.

As per claim 3: Gilbert discusses a method of manufacturing a plurality of the integrated circuits of claim 2, including the steps of: manufacturing a plurality of physical integrated circuits; and **(col.5, lines 21-23)** injecting, into the non-volatile memory of each of the integrated circuits: code for running a software process; and secret information; **(col.4, lines 4-15 and col.6, lines 24-26)** wherein the secret information is positioned in relatively different locations of the non-volatile memories and the code on each integrated circuit is such that the software process of each integrated circuit knows the location in memory via which the secret information is accessible on that integrated circuit. **(col.6, lines 18-22 and col.7, lines 55-65)**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leynna T. Truvan whose telephone number is (571) 272-3851. The examiner can normally be reached on Monday - Thursday (7:00 - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. T. T./
Examiner, Art Unit 2135
/KIMYEN VU/
Supervisory Patent Examiner, Art Unit 2135